Q.P. Code: 19EC4202 **R19**

Reg. No: | | | | | | | | | | |

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY:: PUTTUR

(AUTONOMOUS)

M.Tech I Year I Semester Regular Examinations January 2020

DIGITAL IC DESIGN

(VLSI)

Time: 3 hours Max. Marks: 60

(Answer all Five Units **5 x 12 = 60** Marks)

UNIT-I

1	**a**	Design and explain the operation of 2 input NMOS NAND gate.	**6M**
	b	Compare the characteristics of the different types of MOS inverters in terms of Noise margin and power dissipation.	**6M**
		OR	
2	**a**	Explain the procedure to design an adder circuit using CMOS logic.	**6M**
	b	What are the advantages of dynamic logic over static CMOS logic.	**6M**
		UNIT-II	
3	**a**	Sketch the schematic diagram of a SRAM memory cell along with sense amplifier and data write circuitry.	**8M**
	b	Explain about power consumption in CMOS gates.	**4M**
		OR	
4	**a**	Explain the read and write operations for a one transistor DRAM cell.	**6M**
	b	In what way DRAM's differ from SRAM's.	**6M**
		UNIT-III	
5	**a**	Explain the working principle of Bi-CMOS with the help of static and dynamic characteristics.	**8M**
	b	List the advantages and disadvantages of Bi-CMOS.	**4M**
		OR	
6	**a**	Draw the schematic diagram of different Bi-CMOS inverters and explain their operations.	**8M**
	b	Design NAND gate in Bi-CMOS logic.	**4M**
		UNIT-IV	
7	**a**	What is the need for design rules? Explain.	**5M**
	b	Discuss about 'Mead Conway Design' rules for silicon gate NMOS process.	**7M**
		OR	
8	**a**	Design a CMOS logic gates for the function $F = ((A + BC)D)'$. Also indicate the connections of signals F, V_{DD} and GND. Draw the stick diagram representation for the circuit designed.	**8M**
	b	What are the CMOS based design rules.	**4M**
		UNIT-V	
9	**a**	Draw and explain the Booth Decode cell used for Booth multiplier.	**6M**
	b	Design and explain a 4 Bit CLA Adder.	**6M**
		OR	
10	**a**	How to design the ALU sub-system? Explain steps involved in the design.	**6M**
	b	Design the sub-system serial parallel Multiplier.	**6M**

***** END *****